ULTRAMINIATURE PH ISFET WITH BACK SIDE CONTACTS AND Ta_2O_5 GATE MATERIAL FOR USE IN A GUIDEWIRE TIP

A. Prak[1], H.H. van den Vlekkert[1] and M.-A. Levine[2]
[1] LioniX International, Enschede, the Netherlands
[2] Makaha Medical LLC, Pottstown, PA 19465, USA

ABSTRACT

We fabricated ultraminiature ISFETs with backside contacts and a Ta_2O_5 gate. The chips fits in a catheter tip with an internal diameter of 0.3 mm which will be inserted into the brain vasculature to monitor patients suffering from stroke. To fabricate the ISFET we used through silicon vias based on IceMOS TSV technology, ion implantation and backgrinding, thermal oxidation and Tantalum evaporation and oxidation. The behavior of the vias was as expected. The ISFET were measured on a wafer which has undergone exactly the same processing, except for the vias. The Ta_2O_5 ISFETs have almost Nernstian response and very low drift.

INTRODUCTION

Since the invention of the ISFET (Ion Sensitive Field Effect Transistor) by Bergveld in 1970 [1] a large number of technologies for ISFET fabrication and ISFET applications have been developed. A number of vendors offer ISFETs on the market (e.g. Sentron, Mettler Toledo, Honeywell, Fisher Scientific, Endress + Hauser). Typically, the commercial ISFETs are mounted in a probetip either with or without an integrated reference electrode. ISFETs, being solid state devices, offer advantages over their counterparts, pH glass electrodes, in terms of size, mechanical robustness, chemical resistance and ease of maintenance.

Motivated by the fact that continuous pH monitoring is critical for patients suffering from stroke or severe head injury, we pursue a solution to mount an ISFET in a guidewire tip with an ID (inner diameter) of 300 µm for use in the brain vasculature. A chip of such a small size requires a BSC (back side contact) approach because the packaging of an ISFET with front side contacts would be too space consuming, especially the separation of the part exposed to the sample and the dry, electronic part composing the bondpads.

A number of approaches to fabricate BSC-ISFETs have been published through the years. An overview is given in [2]. Most BSC technologies are based on the anisotropic wet etching of the silicon substrate from the backside to achieve an electrical contact with the bottom of the implanted source and drain regions on the front side. Issues associated with this approach are the process compatibility to a CMOS-grade process, the need to perform lithography on a surface with large topography and the relative large footprint caused by the inclined sidewalls of the anisotropically etched contact holes. These issues also exist in an 'inverted' approach based on bonding and etchback in which the gate is positioned in the etched recess and the electrical contacts are on the front side of the wafer [4,5].

Our requirements of a smaller footprint and a CMOS compatible process forced us to explore the possibilities to realize electrical vias by DRIE (Deep Reactive Ion Etching). DRIE became a mature process when the Bosch process was introduced in the mid-90's by Larmer and Schlip [6]. With the Bosch process, it is possible to realize throughholes in a wafer with almost vertical sidewalls and with a very high aspect ratio by cycling of an etching process based on SF6 and a passivation process based on C_4F_8. To our knowledge, the use of DRIE etching for BSC-ISFETs has been very limited. One example is by Ingebrandt et al. [7]. They realized backside contacts by deep reactive ion etching of circular holes with a diameter of 100-150 µm and doping the sidewalls of the holes by gas phase boron doping from planar diffusion sources. They flip-chip bonded the gold plated back side contacts of the ISFET array on a standard 22 pin DIL package. The chip was extremely delicate because in their process the DRIE stopped on a thin dielectric membrane and the contact holes were not filled.

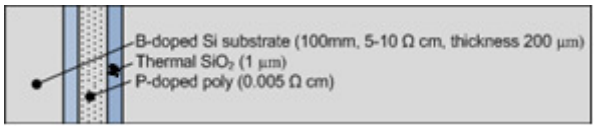
FABRICATION

To fabricate our n-channel BSC-ISFETs we made use of the IceMOS TSV process. IceMOS (Belfast, Northern Ireland) delivered to us a customized substrate with through wafer interconnects of 35 x 70 μm^2 and a resistivity of 0.005 Ω·cm in a p-doped substrate of 5 – 10 Ω·cm. The interconnects are performed using through wafer DRIE etching, sidewall oxidation, and refill of heavily n-doped polysilicon. The substrate is fully CMOS compatible and stable up to temperatures of 1200 ˚C which allows post-via ISFET fabrication including diffusion of source/drain implantations and formation of the gate oxide. After backgrinding to 200 µm and CMP (Optim Wafer Services, Gréasque, France) we obtained substrates as shown in Fig. 2a. To obtain an electric isolation on the backside of the wafer and to form a barrier for the outdiffusion of Phosphorous from the vias during the subsequent high temperature steps, we deposited an SiO_2 layer by LPCVD using TEOS as a precursor (Fig. 2b). Next, a 100 nm screen oxide is grown and wafers undergo Boron and Phosphorous implantations (IBS,

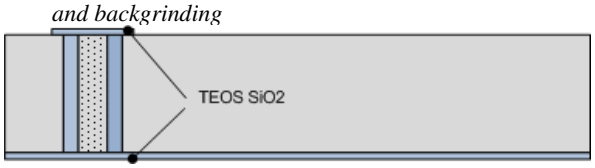
Peynier, France) to define the channel stopper and the source/drain areas (Fig. 2c). To realize the gate, the oxide is etched open and a dry CMOS grade gate oxide is grown (80 nm, 1050 ˚C) followed by evaporation, oxidation and annealing of Ta to obtain an ISFET with Ta_2O_5 as the top gate dielectric (Fig 2d). Ta_2O_5 is a gate dielectric known for its superb properties such as almost Nernstian sensitivity (56-58 mV/pH), wide pH range (pH 2-12) and low drift. Finally, contact holes to the vias (front side as well as back side) and source/drain areas are etched using an RIE process for the Ta_2O_5 layer and a BHF etch for the SiO_2, followed by sputtering and patterning of an aluminum (1% Si) layer for interconnects between the source/drain areas and the vias on the front side and the bondpads on the backside (Fig. 2e). A picture of the ISFET is shown in Fig. 3.

The ISFET chip includes an ESD protection electrode connected to a diode to protect the gate against breakdown as a result of electrostatic charge.

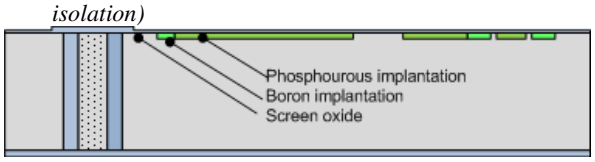
The size of the fabricated chips is 0.23 x 1.00 x 0.20 mm^3 (w x l x t) which results in approx. 20.000 chips on a single 100 mm wafer. As far as we know this is the smallest ISFET chip ever made.



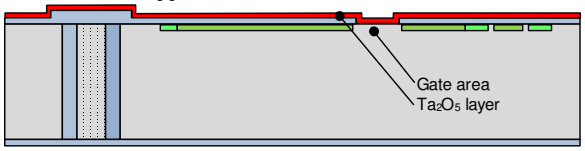
(a) Wafer cross section after realization of interconnects and backgrinding



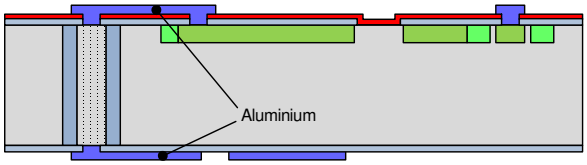
(b) After SiO_2 TEOS deposition (diffusion barrier and isolation)



(c) After implantation the source/ drain areas and the channel stopper



(d) After growing the gate oxide and deposition of Ta_2O_5.



(e) After etching contact holes and aluminum deposition on front side and back side.

Fig. 2. Fabrication process of the BSC-ISFET with Ta_2O_5 gate.

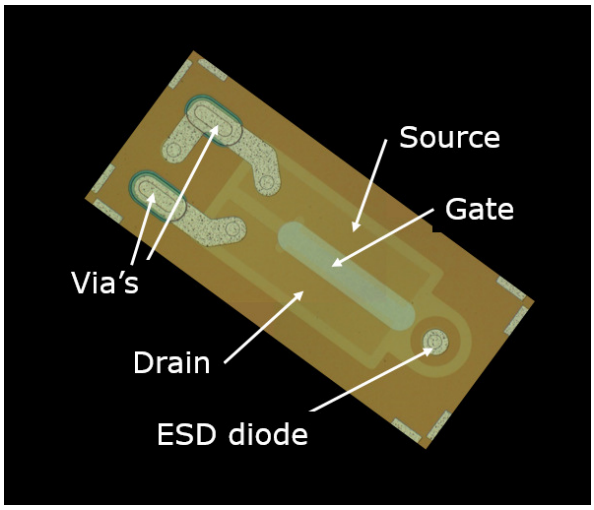


Fig. 2. ISFET chip

RESULTS

Vias

We measured via characteristics such as the via resistance and the isolation of the via from the substrate. Results are shown in Fig. 3.

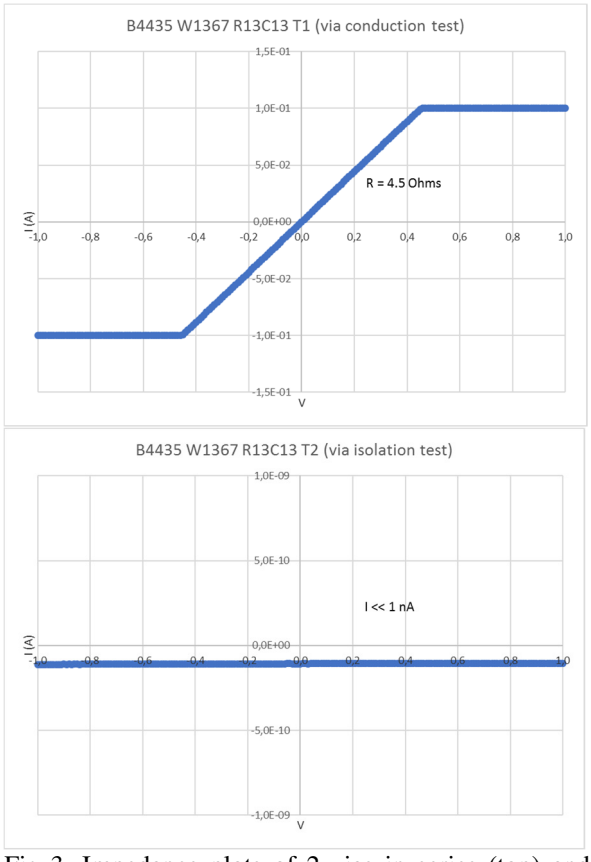


Fig 3. Impedance plots of 2 vias in series (top) and between 2 vias which are not connected, showing that the via resistance is 2,25 Ohms, and the leak current through the liner oxidation < 1 E^{-10} A.

ESD Diode

The diode characteristic of the ESD diode was measured and is shown in fig. 5. The diode closes in the operating range of the ISFET (I leak < 1 nA) and conducts to the substrate at voltages < -0.5 V)

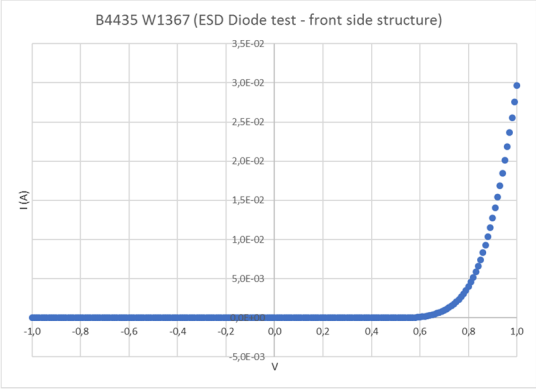


Fig 5. Diode I-V curve of the ESD diode. The leak current in reverse i_{leak} < 1 nA.

MOSFET

The FETs on the wafer were not working as we expected. After investigating the process and equipment carefully, we found that a cross contamination had occurred in one of the furnaces, resulting in a slight n-doping on the surface of the wafer, including the channel area of the FET which is supposed to be p-doped. In the past we have fabricated identical Ta_2O_5 ISFETs without vias which not suffered from this problem, and therefore we will show the results of those MOSFETS and ISFETs. We expect to obtain the same results from the wafers with vias once the cross-contamination issue has been solved.

Fig 6 shows the Vg-Ids curves of a number of MOSFETs at Vds = 0.5 V. The curves show a very steep response in the threshold region, opening at Vg = 0V and (Ids < 0,1 µA) and having their working point (1 ds = 100 µA) at Vg = 0.5 V.

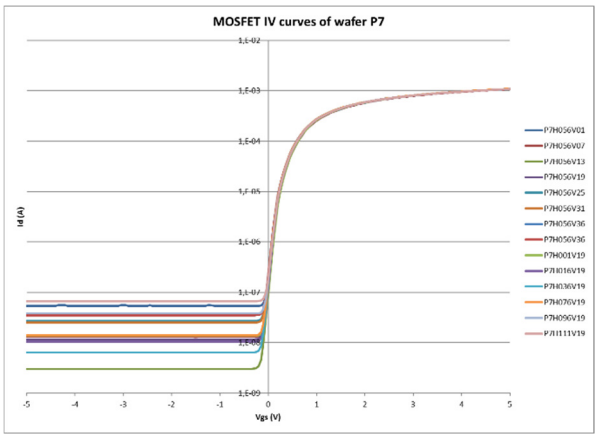


Fig 6. Vg-Ids curves of a number of MOSFETs at Vds = 0.5 V.

ISFET

We measured the most important ISFET characteristics: sensitivity, drift and dVgs/dT as follows:

We mounted 7 ISFETs on a dipstick by means of an epoxy, completely covering the chips and wirebonds, leaving only open the gate area. We measured the ISFET against an Ag / AgCl reference electrode in a temperature controlled bath. The used ISFET Amplifier (type source follower, manufactured by P. Bergveld) was used at operating conditions Vds = 0.5V and Ids= 100 µA. The common Ag/AgCl was kept at ground, and Vgs was used as the readout signal. The Amplifier is capable of controlling 10 channels simultaneously.

The sensitivity was measured by immersing the ISFETs in buffers of pH 4, 7 and 10 and allowing sufficient time for stabilization of the temperature (30 ˚C). We found a sensitivity of almost 59 mV/ pH at 30 ˚C which is close to the maximum set by the Nernst Equation.

The drift was measured by monitoring the gate - source voltage during 72 hours at constant temperature in the dark. We observed a drift of some mV in the first 6 hours, which reduced to less than 1 mV between 6 and 72 hours (fig. 7.

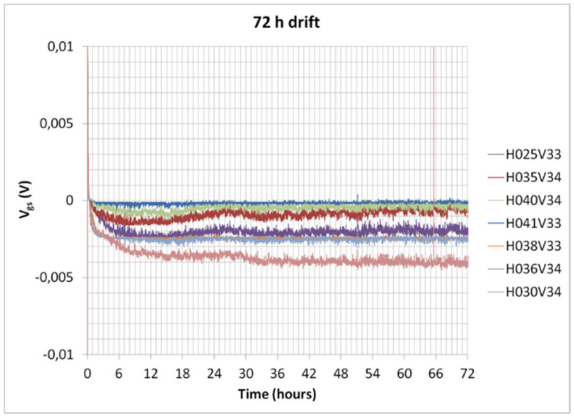


Fig 7. Measured drift rate of 7 ISFETs

At the used setting of Id = 100 µA, the response Vgs depends on temperature. An operating point for which Vgs / dT = 0 results in an ISFET with zero temperature effect on the read-out value, which obviously has many advantages. To find the isothermal operating point we varied Ids from 10 to 100 µA in 5 steps and Vds from 0.1 to 1.0 V (4 steps). For each combination of Id and Vds we measured the response to pH7 at 30 and at 40 ˚C. We found the isothermal operating point at Id = 20 µA being independent of Vds (Fig 8.).

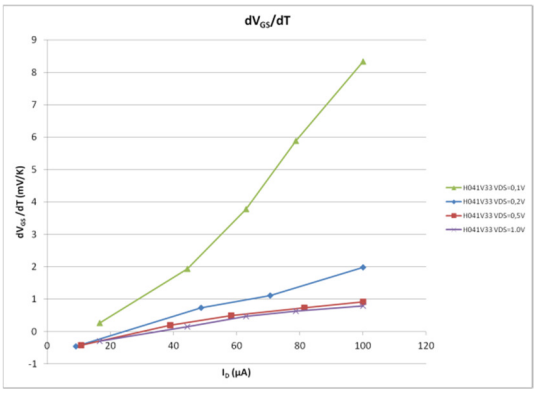


Fig 8. Temperature dependence of the read-out signal Vgs at various values of Id and Vds (--Vds=0.1V; -- Vds=0.2V; -- Vds=0.5V;-- Vds=1.0V).

The measured ISFET characteristics are summarized in Table 1.

Table 1. ISFET characteristics

Parameter	**Value**
Sensitivity (pH 4-10, T=30˚C)	58.8 ± 0.2 mV/pH
Offset (pH 7, T=30˚C)	332 ± 50 mV
Drift (0 to 6h)	0.2 ± 0.2 mV
Drift rate (6 to 72h)	< 0.02 mV/h
Isothermal current (dVg/dT =0)	Id = 20 µA

CONCLUSIONS

We fabricated miniature ISFETs with backside contacts to be used in a guidewire tip which will be inserted into the brain vasculature of patients suffering from stroke.

The first process run of these ISFETs was only partially successful because a cross contamination issue in one of the furnaces occurred and caused a shallow doping of the n-type in the p-channel, preventing the ISFETs to work.

Measurements on ISFETs from a similar wafer with an identical ISFET process, but without the vias show very good characteristics: Sensitivity 59 mV /pH at 30 ˚C, drift < 0.02 mV/h after stabilization of 6h and an isothermal operating point at Ids = 20 µA.

REFERENCES

[1] Bergveld P. Development of an Ion-Sensitive Solid-State Device for Neurophysiological Measurements. *IEEE Trans. Biomed. Eng*. 1970
[2] Cane C., Gracia I., Merlos A. Microtechnologies for pH ISFET Chemical Sensors. Microelectron. J. 1997;28(4):389–405.
[3] H.H. Van den Vlekkert, B. Kloeck, D. Prongue, J. Berthoud, B. Hu, N.F. de Rooij, E. Gilli and P.H. de Crousaz, A pH-ISFET and an integrated pH-pressure sensor with back-side contacts, Sensors & Actuators, 14, (1988) 165-176.
[4] H. Yagi and T. Sakai, Rear-gate ISFET with a membrane locking structure using an ultrahigh concentration selective boron diffusion technique, Sensors &Actuators B, 13-14 (1993) 212-216.
[5] A.S. Poghossian, Method of fabrication of ISFETs and CHEMFETs on a SiSiOESi structure, Sensors & Actuators B, 13-14 (1993) 653-654.
[6] F. Lärmer, A. Schlip, A Method of Anisotropically Etching Silicon, Licensed from Robert Bosch GmbH: US Patent No. 5,501,893 (1996).
[7] S. Ingebrandt, C.K. Yeung, W. Staab, T. Zetterer, A. Offenhausser, Backside contacted field effect transistor array for extracellular signal recording, Biosensors and Bioelectronics 18 (2003), 429-435.